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Date:	April 18, 2005	Phone Number	Fax Number
To:	Board of Patent Appeals & Interferences		(703) 872-9306
From:	Kevin J. Zilka		

Docket No.:   NVIDP033A/P000873   **App. No.: 10/657,957**

Total Number of Pages Being Transmitted, Including Cover Sheet: 27

Message:

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Kevin J. Zilka

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April 18, 2005

Practitioner's Docket No. NVIDP033A/P000873   *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: James M. Van Dyke et al.

Application No.: 10/657,957	Group No.: 2186
Filed: 09/08/2003	Examiner: Choi, Woo H.

For: SYSTEM AND METHOD FOR A HIGH BANDWIDTH-LOW LATENCY MEMORY CONTROLLER

Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION--37 C.F.R. § 1.192)

1.   Transmitted herewith is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on February 18, 2005.

2.   STATUS OF APPLICANT

       This application is on behalf of other than a small entity.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*
(When using Express Mail, the Express Mail label number is mandatory;
Express Mail certification is optional.)

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Date: 4/18/2005

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Erica L. Farlow

(type or print name of person certifying)

* Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.

Transmittal of Appeal Brief--page 1 of 2

3. FEE FOR FILING APPEAL BRIEF

    Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

    other than a small entity $500.00

    Appeal Brief fee due $500.00

4. EXTENSION OF TERM

    The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

    Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

    The total fee due is:

    Appeal brief fee $500.00
    Extension fee (if any) $0.00

    TOTAL FEE DUE $500.00

6. FEE PAYMENT

    Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 50-1351 (Order No. NVIDP033A).

    A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

    If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NVIDP033A).

    _____
    Signature of Practitioner
    Kevin J. Zilka
    Zilka-Kotab, PC
    P.O. Box 721120
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Transmittal of Appeal Brief—page 2 of 2

PAGE 3/27 * RCVD AT 4/18/2005 7:53:42 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/1 * DNIS:8729306 * CSID:408 971 4660 * DURATION (mm-ss):07-30

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PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: James M. Van Dyke et al.

Application No.: 10/657,957   Group No.: 2186
Filed: 09/08/2003   Examiner: Choi, Woo H.
For: SYSTEM AND METHOD FOR A HIGH BANDWIDTH-LOW LATENCY MEMORY
CONTROLLER

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Date: 4/18/2005

Signature

Erica L. Farlow

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* Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or
transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to
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Transmittal of Appeal Brief--page 1 of 2

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Appeal Brief fee due $500.00

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Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5.   TOTAL FEE DUE

The total fee due is:

Appeal brief fee $500.00
Extension fee (if any) $0.00

TOTAL FEE DUE $500.00

6.   FEE PAYMENT

Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 50-1351 (Order No. NVIDP033A).

A duplicate of this transmittal is attached.

7.   FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NVIDP033A).

Reg. No.: 41,429
Tel. No.: 408-971-2573
Customer No.: 28875

Signature of Practitioner
Kevin J. Zilka
Zilka-Kotab, PC
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San Jose, CA 95172-1120
USA

Transmittal of Appeal Brief—page 2 of 2

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Practitioner's Docket No. NVIDP033A/P000873   *PATENT*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: James M. Van Dyke et al.

Application No.: 10/657,957   Group No.: 2186
Filed: September 8, 2003   Examiner: Choi, Woo H.
For: SYSTEM AND METHOD FOR A HIGH BANDWIDTH-LOW LATENCY
       MEMORY CONTROLLER

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on February 18, 2005.

The fees required under § 1.17, and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(i)):

I	REAL PARTY IN INTEREST
II	RELATED APPEALS AND INTERFERENCES
III	STATUS OF CLAIMS
IV	STATUS OF AMENDMENTS
V	SUMMARY OF CLAIMED SUBJECT MATTER
VI	ISSUES
VII	ARGUMENTS
VIII	APPENDIX OF CLAIMS INVOLVED IN THE APPEAL

-2-

IX   APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE
        APPELLANT IN THE APPEAL

The final page of this brief bears the practitioner's signature.

-3-

I REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is NVIDIA Corporation.

-4-

11 RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no other such appeals, interferences, or related judicial proceedings.

Since no such proceedings exist, no Related Proceedings Appendix is appended hereto.

-5-

III STATUS OF CLAIMS (37 C.F.R. § 41.37(c) (1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-27

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims withdrawn from consideration: none
2. Claims pending: 1-27
3. Claims allowed: 24
4. Claims rejected: 1-23 and 25-27

C. CLAIMS ON APPEAL

The claims on appeal are: 1-23 and 25-27

See additional status information in the Appendix of Claims.

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IV STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

As to the status of any amendment filed subsequent to final rejection. such
amendment was not entered.

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V SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

With respect to a summary of Claim 1 et al., a memory controller system is provided. As set forth in Figure 1B and the accompanying description of pages 8 and 9 of the originally-filed specification, a plurality of memory controller subsystems are coupled to a plurality of computer components. Further, each memory controller subsystem includes at least one read or write queue with an input coupled to one of the computer components and an output coupled to memory for queuing read or write commands to be sent to the memory, and at least one activate queue with an input coupled to one of the computer components and an output coupled to the memory for queuing activate commands to be sent to the memory. Still yet, as set forth in the first paragraph of page 17 of the originally filed specification, the activate commands are capable of being restored to a row and a bank associated with the read or write commands at a head of the associated read or write queue.

With respect to a summary of Claim 25 et al., a memory controller system is provided including at least three memory controller subsystems coupled to a plurality of computer components. As set forth in Figure 1B and the accompanying description of pages 8 and 9 of the originally-filed specification, a first one of the memory controller subsystems is coupled only to a graphics unit computer component, a second one of the memory controller subsystems is coupled only to a central processing computer component, and a third one of the memory controller subsystems is coupled only to a display refresh module computer component.

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VI ISSUES (37 C.F.R. § 41.37(c)(1)(vi))

Following, under each issue listed, is a concise statement setting forth the corresponding ground of rejection.

Issue # 1: The Examiner has rejected Claims 1-9, 11-13, 15-23, and 26-27 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622.225, hereinafter "Kessler").

Issue # 2: The Examiner has rejected Claim 14 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"), and further in view of Dell et al. (US Patent Application Publication No.: 2001/0000822, hereafter "Dell").

Issue # 3: The Examiner has rejected Claim 10 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"), and further in view of Margulis (US Patent No. 6,057,862, hereinafter "Margulis").

Issue # 4: The Examiner has rejected Claim 25 under 35 U.S.C. 102(e) as being anticipated by Margulis (US Patent No. 6,057,862, hereinafter "Margulis").

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VII ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

The claims of the groups noted below do not stand or fall together. In the present section, appellant explains why the claims of each group are believed to be separately patentable.

Issue #1:

The Examiner has rejected Claims 1-9, 11-13, 15-23, and 26-27 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler").

Group #1: Claims 1-9, 11-13, 15-23, and 27

Specifically, the Examiner continues to rely on the following excerpt from Kessler to make a prior art showing of appellant's claimed "wherein the memory controller is capable of restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue" (see all independent claims, except Claims 24-25).

> "A computer system includes a memory controller interfacing
> the processor to a memory system. The memory controller
> supports a memory system with a plurality of memory devices,
> with multiple memory banks in each memory device. The memory
> controller supports simultaneous memory accesses to different
> memory banks. Memory bank conflicts are avoided by examining
> each transaction before it is loaded in the memory transaction
> queue. On a first clock cycle, the new pending memory request
> is transferred from a pending request queue to a memory
> mapper. On the subsequent clock cycle, the memory mapper
> formats the pending memory request into separate signals
> identifying the DEVICE, BANK, ROW and COLUMN to be accessed by
> the pending transaction. In the next clock cycle, the DEVICE

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> and BANK signals are compared with every entry in the memory
> transaction queue to determine if a bank conflict exists. If
> so, the new memory request is rejected and recycled to the
> pending request queue." (see Abstract)

In response to appellant's previous arguments, the Examiner now notes appellant's use of "capable of being" language in the context of the above claim language. Specifically, the Examiner stated that such language does not claim an act or a structure that actually restores. Appellant respectfully disagrees.

The Examiner continues by arguing that Novak "has the capability to actually issue activate commands to a row and a bank associated with the read or write commands and the same structure is capable of supporting restoration of an activate command." Moreover, the Examiner continues by arguing that "[a]n activate command to a row and a bank is brought back into existence along with other appropriate primitive commands (i.e. precharge, read/write) when a recycled memory request gets decoded again in an attempt to access the memory again."

Appellant respectfully disagrees with these assertions. First, the Examiner has stated that "[n]or does Novak disclose that the activate commands are capable of being restored to a row and a bank associated with the read or write command at a head of the associated read or write queue," and the Examiner states that he is relying on Kessler to meet such limitation. Thus, it appears that the Examiner is making conflicting statements, namely admitting that Novak does not disclose the claim limitations at issue, and then asserting that they are met by Novak.

Further, the Examiner's assertions are baseless, as no excerpts have been cited. Still yet, the Examiner's statements are simply incorrect. For example, the Examiner states that Novak "is capable of supporting restoration of an activate command." After carefully reviewing the entire Novak reference, this is simply incorrect.

Still yet, the Examiner continues to support his position by stating that appellant's

-11-

claim limitations are met "when a recycled memory request gets decoded again in an attempt to access the memory again." Again, after carefully reviewing the entire Novak reference, there is absolutely no mention of "recycling" any memory request. Further, even if there were such a suggestion, it would be improper to leap to the conclusion that Novak even suggests appellant's claimed "restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue."

Since no specific prior art showing has been made, it appears that the Examiner is relying on an inherency argument regarding the above emphasized claim limitations. In view of the arguments made hereinabove, any such inherency argument has been adequately rebutted, and a notice of allowance or a specific prior art showing of such claim features, in combination with the remaining claim elements is respectfully requested. (See MPEP 2112)

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on appellant's disclosure. *In re Vaeck*,947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Appellant respectfully maintains that the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to at least suggest **all** of appellant's claim limitations.

> *Group #2: Claim 26*

-12-

With respect to the current grouping, the Examiner relies on the following excerpt from Novak to meet appellant's claimed "wherein the restoring utilizes a field in the read or write queue that contains an activate write address" (see Claim 26).

Fig. 7

First, Novak does not suggest any restoring of an activate command, and thus inherently can not meet the present claim limitations. Further, after carefully reviewing the above figure, it is clear that there is simply no restoring that specifically utilizes a field in the read or write queue that contains an activate write address.

-13-

Again, appellant respectfully maintains that the third element of the *prima facie* case of obviousness has not been met. since the prior art references, when combined, fail to at least suggest **all** of appellant's claim limitations.

Issue #2

The Examiner has rejected Claim 14 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"), and further in view of Dell et al. (US Patent Application Publication No.: 2001/0000822, hereafter "Dell").

Group #1: Claim 14

Appellant respectfully disagrees with this rejection, as it would be unobvious to combine Dell with the remaining references, as suggested by the Examiner.

Issue #3

The Examiner has rejected Claim 10 under 35 U.S.C. 103(a) as being unpatentable over Novak et al. (US Patent No. 6,295,586, hereinafter "Novak") in view of Kessler et al. (US Patent No. 6,622,225, hereinafter "Kessler"), and further in view of Margulis (US Patent No. 6,057,862, hereinafter "Margulis").

Group #1: Claim 10

Appellant respectfully disagrees with this rejection, as Margulis simply does not meet appellant's "wherein the computer components include a central processing unit, a display refresh module, and a graphics unit," in the context claimed. Yet gain, appellant respectfully maintains that the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to at least suggest **all** of appellant's claim limitations.

-14-

Issue #4

The Examiner has rejected Claim 25 under 35 U.S.C. 102(e) as being anticipated by Margulis (US Patent No. 6,057,862, hereinafter "Margulis").

Group #1: Claim 25

Specifically, the Examiner has modified the excerpts he relies upon to reject such claim. In particular, the Examiner now relies on the following excerpts from Margulis to meet appellant's claimed "at least three memory controller subsystems".

FIG. 8

FIG. 9
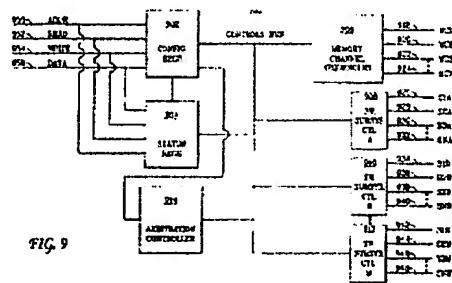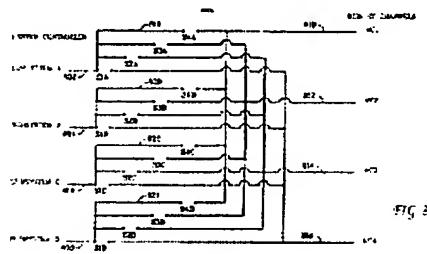
Specifically, the Examiner points to items 802-808 and 908-912 to meet appellant's claimed "at least three memory controller subsystems." First, items 802-808 are mere "subsystems" (i.e. display, CPU, etc.) per the specification of Margulis. Further, items 908-912 in no way meet appellant's claimed "wherein a first one of the memory controller subsystems is coupled only to a graphics unit computer component, a second one of the memory controller subsystems is coupled only to a central processing computer component, and a third one of the memory controller subsystems is coupled only to a display refresh module computer component" (emphasis added).

-15-

It is clear from both Fig. 8 and Fig. 9 that any components therein which may allegedly be considered "at least three memory controller subsystems" are coupled to all of the computer components, and thus do not meet a first one of the memory controller subsystems coupled only to a graphics unit computer component, a second one of the memory controller subsystems coupled only to a central processing computer component, and a third one of the memory controller subsystems coupled only to a display refresh module computer component, as claimed.

Only appellant teaches and claims that each memory subsystem is coupled only to one computer component.

In view of the remarks set forth hereinabove, all of the independent claims are deemed allowable, along with any claims depending therefrom.

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VIII APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal (along with associated status information) is set forth below:

1.   (Original) A memory controller system, comprising:

a plurality of memory controller subsystems coupled to a plurality of computer components, each memory controller subsystem including:

at least one read or write queue with an input coupled to one of the computer components and an output coupled to memory for queuing read or write commands to be sent to the memory, and

at least one activate queue with an input coupled to one of the computer components and an output coupled to the memory for queuing activate commands to be sent to the memory;

wherein the activate commands are capable of being restored to a row and a bank associated with the read or write commands at a head of the associated read or write queue.

2.   (Original) The memory controller system as recited in claim 1, wherein the computer components are selected from the group consisting of a central processing unit, a display refresh module, and a graphics unit.

3.   (Original) The memory controller system as recited in claim 1, wherein the memory includes dynamic random access memory (DRAM).

4.   (Original) The memory controller system as recited in claim 1, wherein the memory includes synchronous dynamic random access memory (SDRAM).

5.   (Original) The memory controller system as recited in claim 1, wherein each memory controller subsystem further includes a multiplexer having inputs coupled

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to the outputs of the read or write queue, and activate queue, the multiplexer further
including an output coupled to the memory.

6.   (Original) The memory controller system as recited in claim 1, wherein the read or
write commands, and the activate commands of each memory controller subsystem
are loaded independent of the state of the memory.

7.   (Original) The memory controller system as recited in claim 1, wherein the
commands are loaded in at least one of the queues of each memory controller
subsystem based on rows and banks of references in at least one of the queues.

8.   (Original) The memory controller system as recited in claim 1, wherein the loading
of the commands in at least one of the queues of each memory controller subsystem
is delayed based on rows and banks of references in at least one of the queues.

9.   (Original) The memory controller system as recited in claim 1, wherein each read or
write queue is permitted to queue commands for only a single row in each bank.

10.   (Original) The memory controller system as recited in claim 1, wherein the
computer components include a central processing unit, a display refresh module,
and a graphics unit.

11.   (Original) The memory controller system as recited in claim 1, wherein the memory
controller system arbitrarily selects to unload commands from queues associated
with any of the computer components.

12.   (Original) A method for controlling memory utilizing a memory controller,
comprising:
          receiving a plurality of read or write commands, and activate commands
from a plurality of queues capable of being loaded from a plurality of computer
components;

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arbitrating the delivery of the read or write commands, and activate commands from the queues to the memory; and

delivering the arbitrated read or write commands, and activate commands to the memory;

wherein the memory controller is capable of restoring the activate commands to a row and a bank associated with the read or write commands at a head of a read or write queue.

13.   (Original) The method as recited in claim 12, wherein the computer components are selected from the group consisting of a central processing unit, a display refresh module, and a graphics unit.

14.   (Original) The method as recited in claim 12, wherein the memory includes dual data rate (DDR) memory.

15.   (Original) The method as recited in claim 12, wherein the memory includes dynamic random access memory (DRAM).

16.   (Original) The method as recited in claim 12, wherein the memory includes synchronous dynamic random access memory (SDRAM).

17.   (Original) The method as recited in claim 12, wherein the delivery of the read or write commands, and activate commands from the queues to the memory is arbitrated utilizing a timer.

18.   (Original) The method as recited in claim 17, wherein the timer arbitrates the delivery of the commands to ensure that sequential commands are delivered sequentially.

-19-

19.   (Original) The method as recited in claim 12, wherein the delivery of the read or
        write commands, and activate commands from the queues to the memory is
        arbitrated based on a predetermined order.

20.   (Original) The method as recited in claim 12, wherein the delivery of at least one of
        the commands is arbitrated based on a bank and a row at a head of the queues.

21.   (Original) The method as recited in claim 12, wherein the delivery of at least one of
        the commands is arbitrated based on the read or write commands.

22.   (Original) The method as recited in claim 19, wherein the predetermined order
        prioritizes the computer components.

23.   (Original) The method as recited in claim 19, wherein the predetermined order
        prioritizes the read or write commands, the activate commands.

24.   (Previously Amended) A method, comprising:
               providing at least three parallel-coupled memory controller subsystems each
        capable of:
               queuing read or write commands to be sent to the memory in at least one
        read or write queue with an input coupled to a computer component and an output
        coupled to memory, and
               queuing activate commands to be sent to the memory in an activate queue
        with an input coupled to the computer component and an output coupled to the
        memory,
               wherein a first one of the memory controller subsystems is coupled only to a
        graphics unit computer component, a second one of the memory controller
        subsystems is coupled only to a central processing computer component, and a third
        one of the memory controller subsystems is coupled only to a display refresh module
        computer component.

-20-

25.   (Previously Amended) A memory controller system, comprising:

           at least three memory controller subsystems coupled to a plurality of
computer components;

           wherein a first one of the memory controller subsystems is coupled only to a
graphics unit computer component, a second one of the memory controller
subsystems is coupled only to a central processing computer component, and a third
one of the memory controller subsystems is coupled only to a display refresh module
computer component.

26.   (Previously Presented) The memory controller system as recited in claim 1, wherein
the restoring utilizes a field in the read or write queue that contains an activate write
address.

27.   (Previously Presented) The memory controller system as recited in claim 26,
wherein the activate write address is indicated by a write pointer when the activate
queue is written.

IX APPENDIX LISTING ANY EVIDENCE RELIED ON BY THE APPELLANT IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(ix))

There is no such evidence.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP033A).

Respectfully submitted,

By: _____   Date: ____4/18/05____
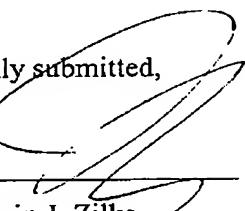
Kevin J. Zilka

Reg. No. 41,429
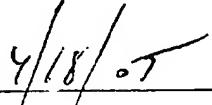
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